REMARKS/ARGUMENTS

Brief Summary of Status

Claims 1-184 are pending in the application.

Claims 80-112, and 129-133 are allowed.

Claims 1-79, 113-128, and 134-184 are rejected.

Claim Rejections - 35 U.S.C. § 102

3. In the office action, the Examiner states:

"Claims 1-2, 6-8, 12-15, 17, 20-21, 25, 27, 30, 34, 37, 113, 116-117, 119, 121, 123, 126-127, 134-135, 139-141, 145-146, 148-150, 153-154, 158, 160, 163, 170 are rejected under 35 U.S.C. 102(b) as being anticipated by Alelyunas et al (5,705,949)." (hereinafter referred to as "Alelyunas") (office action, Part of Paper No./Mail Date 20070430, p. 2).

4. In the office action, the Examiner states:

"Claims 1-8, 12-27, 34, 37-41, 113, 116-117, 119, 121, 123, 126-127, 134-141, 145-146-160, 163, 167, 170-175, 178, 183, 184 are rejected under 35 U.S.C. 102(b) as being anticipated by Kost et al. (6,081,215)." (hereinafter referred to as "Kost") (office action, Part of Paper No./Mail Date 20070430, p. 4).

5. In the office action, the Examiner states:

"Claims 42-57, 62-69, 76-79, 113-128, 176, 177, 179-182 are rejected under 35 U.S.C. 102(b) as being anticipated by Kost et al. (6,081,215)." (hereinafter referred to as "Kost") (office action, Part of Paper No./Mail Date 20070430, p. 5).

Claim Rejections - 35 U.S.C. § 103

7. In the office action, the Examiner states:

"Claims 9-11, 28-33, 59-61, 72-75, 142-144, 161-162, 164-166 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kost in view of Stewart (5,671,253)." (hereinafter referred to as "Kost" and "Stewart", respectively) (office action, Part of Paper No./Mail Date 20070430, p. 6).

Allowable Subject Matter

7. In the office action, the Examiner states:

"Claims 129-133 are allowed." (office action, Part of Paper No./Mail Date 20061002, p. 4).

Claim Rejections - 35 U.S.C. § 102

3. In the office action, the Examiner states:

"Claims 1-2, 6-8, 12-15, 17, 20-21, 25, 27, 30, 34, 37, 113, 116-117, 119, 121, 123, 126-127, 134-135, 139-141, 145-146, 148-150, 153-154, 158, 160, 163, 170 are rejected under 35 U.S.C. 102(b) as being anticipated by Alelyunas et al (5,705,949)." (hereinafter referred to as "Alelyunas") (office action, Part of Paper No./Mail Date 20070430, p. 2).

The Applicant respectfully traverses.

The Applicant respectfully points out that, in order to support a proper rejection under 35 U.S.C. §102, a singular reference must teach and disclose each and every limitation of the subject matter as claimed by the Applicant. If the singular reference fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant, the rejections under 35 U.S.C. § 102 should be withdrawn.

The Applicant has amended certain of the claims.

With respect to Applicant amendments to the claims, the Applicant respectfully refers the Examiner to at least FIG. 5A, FIG. 5B, FIG. 6, FIG. 7, FIG. 8 and so on and their respective written description portions wherein selectivity and adaptability are disclosed in which the DSP is operable to perform the actual compensation and/or the DSP is also operable to the direct another module (e.g., an ADC) to perform a compensation operation. The Applicant respectfully asserts that the Applicant teaches and discloses in numerous embodiment in the originally submitted specification (including written description and figures) how the compensation operation can be performed only in the DSP, how alternatively the DSP can direct another module (e.g., an ADC) to perform a compensation operation, and/or how a combination of these two types of compensation can be performed. In other words, there is selectivity in which manner the compensation operation is to be performed.

The Applicant respectfully points out that Alelyunas fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant.

The Examiner also asserts:

"Consider claim 1 and 1 13,134,163 as claimed now. Alelyunas discloses a receiver comprising an analog to digital converter (14) that generates digital samples of

the modulated data coupled to a digital signal processor (16). The DSP determines compensation operations to be performed by the receiver on the digital samples(Id,Qd) of the modulated serial data. The DSP demodulated(decode) the digital samples to extract the digital data (I and Q) (see fig.l) The DSP interfaces two devices (12,14) communicatively coupled via at least one of twisted pair cable, a coaxial cable and a twin ax cable as claimed in claim 2. The DSP determines a compensation operation to be performed on the digital data (Id,Qd) as claimed in claim 12,116,135,145. The DSP is implemented in a data communication application as claimed in claim 13 and 146. (see abstract and col.2, lines 53-67 and col. 3, lines 20-37) The DSP selects at least one compensation option from the plurality of compensation options to ensure the proper characteristics of the digital data and the proper characteristic of the digital data comprises at least one of gain, a phase and an offset 'as claimed in claims 14-1 5 and 17 and 117 and 148,150 (see abstract and col.2, lines 53-67). The DSP determines compensation to be performed to substantially eliminate a pattern of noise introduced during the digital sampling of the analog data by the A/D converter to generate the digital data as claimed in claims 6-8 and 139-141(see col.3, lines 10-16). The analog to digital converter comprises a plurality of A/D (14) converters performing digital sampling of the incoming data signal as claimed in claim 20-21 ,1 19,121 and 153-1 54. The analog data is partitioned into plurality of channels (I, Q) each channel of the plurality of channels communicatively coupled to one A/D converter (14) and the analog signal is simultaneously fed to each A/D converter within the plurality of A/D converters as claimed in claims 25, 27 and 119,121,123,126-127 and 158 and 160, The DSP is operable to perform digital signal processing on the digital (Id, Qd) data to ensure the proper characteristic of the digital data as claimed in claim 37,170. The I and Q signal output of from DSP are decoded to generated the transmitted signal as claimed in claims 30 and 163." (office action, Part of Paper No./Mail Date 20070430, p. 2-3)

The Applicant respectfully believes that Alelyunas teaches and discloses performing compensation only in the DSP described therein. The Applicant is unable to find any indication within Alelyunas that any compensation is operable to be performed anywhere except within the DSP described therein. The Applicant respectfully believes that Alelyunas fails to teach and disclose performing compensation in any other module,

functional block, device, etc. that is coupled to the DSP, and the Applicant respectfully believes that Alelyunas fails to teach and disclose selectively performing the compensation in either the DSP or any other module, functional block, device, etc. that is coupled to the DSP. Since Alelyunas teaches and discloses performing compensation only in the DSP described therein, then there is therefore no

Alelyunas teaches and discloses:

"The DSP compensates for the quadrature phase errors by calculating a compensation matrix which is independent of the frequency of the carrier and applies the compensation matrix to the I' and Q' digital signals." (Alelyunas, within ABSTRACT, emphasis added)

Alelyunas also teaches and discloses:

"The DSP compensates for differential D.C. offset errors by averaging the incoming I.sub.d and Q.sub.d digital signals and subtracting from them an expected value of differential D.C. offset, for example, computed from the long term average of the I.sub.d and Q.sub.d signals, to create offset corrected signals I' and Q'. The DSP compensates for the differential gain imbalance errors by calculating a root means square average of the I' and Q' digital signals and applying to them compensation coefficients K.sub.x and K.sub.y determined from this RMS average, or from a Stochastic Gradient Algorithm, to create I" and Q" signals. The DSP compensates for the quadrature phase errors by calculating a compensation matrix which is independent of the frequency of the carrier and applies the compensation matrix to the I" and Q" digital signals. After performing the above compensation functions, the DSP generates I'" and Q'" output signals which include compensation for the differential offset, differential gain and quadrature phase errors." (Alelyunas, col. 2, line 61 to col. 3, line 7, emphasis added)

When referring to the one and only figure shown therein, Alelyunas teaches and discloses "reference will be made to the appended drawing FIGURE, which, shows a block diagram of a preferred digital signal processing compensator arrangement for a complex receiver that takes I and Q signals, detects and compensates for gain, offset and quadrature errors in the I and Question signals, and generates substantially error-free I'" and Q'" output signals." (Alelyunas, col. 3, lines 10-16 within "BRIEF DESCRIPTION OF THE DRAWING", emphasis added)

As can be seen, it is the "DSP" of Alelyunas that "compensates for" "differential D.C. offset errors", "differential gain imbalance errors", and "quadrature phase errors".

Alelyunas even refers to the "preferred digital signal processing compensator arrangement" that is operable to perform BOTH the detection and compensation (i.e., "detects and compensates") of a number of possible errors.

In other areas, Alelyunas even refers the "DSP" as a "compensator".

Alelyunas also teaches and discloses:

"The I and Q output signals from the complex receiver are converted to digital signals by an A/D converter 14, and are then supplied to a digital signal processor (DSP) referred to herein as a "compensator" 16. After compensation within the compensator 16, and referring to the far right portion of the illustration, the compensator 16 outputs digital I'" and Q'" signals on output busses 18A and 18B for subsequent use and processing by the DSP 16, or other circuitry in a manner well known in the art.

In the FIGURE, in one possible embodiment of the invention the complex receiver 12 and compensator 16 are incorporated into a cell phone, or, alternatively, a cell-phone modem. The system 10 uses complex (I/Q) modulation and demodulation techniques for generating and receiving frequency modulated or FM signals. Preferably, the modulating and demodulating is done mathematically, using the DSP compensator 16, as opposed to analog methods." (Alelyunas, col. 3, lines 28-45, emphasis added)

As can be seen, Alelyunas interchangeably refers to reference numeral 16 as either the "compensator 16" or "DSP compensator 16".

It appears to the Applicant that any compensation is performed exclusively within the "DSP" of Alelyunas. The Applicant respectfully believes that Alelyunas teaches and discloses that any compensation operation is performed exclusively within the "DSP" as a "compensator", or "compensator 16" or "DSP compensator 16".

As such, the Applicant respectfully believes that Alelyunas fails to teach and disclose any performing of any compensation operation outside of the "compensator 16" or "DSP compensator 16". The Applicant also respectfully believes that Alelyunas fails to teach and disclose any performing of any compensation operation outside of the "compensator 16" or "DSP compensator 16" as being directed by the "compensator 16" or "DSP compensator 16" as well.

As such, the Applicant respectfully believes that Alelyunas fails to teach and disclose any selectivity of performing any compensation operation by the digital signal processor or by at least one additional module that is coupled to the digital signal processor.

Therefore, in light of at least these comments made above, the Applicant respectfully believes that Alelyunas fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant in each of independent claims indicated above that the Examiner rejects as being anticipated by Alelyunas.

The Applicant also respectfully believes that the dependent claims indicated above that the Examiner rejects as being anticipated by Alelyunas, being further limitations of the subject matter as claimed in allowable independent claims are also allowable.

As such, in light of at least these comments made above, the Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-2, 6-8, 12-15, 17, 20-21, 25, 27, 30, 34, 37, 113, 116-117, 119, 121, 123, 126-127, 134-135, 139-141, 145-146, 148-150, 153-154, 158, 160, 163, 170 under 35 U.S.C. § 102(b) as being anticipated by Alelyunas.

4. In the office action, the Examiner states:

"Claims 1-8, 12-27, 34, 37-41, 113, 116-117, 119, 121, 123, 126-127, 134-141, 145-146-160, 163, 167, 170-175, 178, 183, 184 are rejected under 35 U.S.C. 102(b) as being anticipated by Kost et al. (6,081,215)." (hereinafter referred to as "Kost") (office action, Part of Paper No./Mail Date 20070430, p. 4).

The Applicant respectfully traverses.

The Applicant has amended certain of the claims.

The Applicant respectfully points out that, in order to support a proper rejection under 35 U.S.C. §102, a singular reference must teach and disclose each and every limitation of the subject matter as claimed by the Applicant. If the singular reference fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant, the rejections under 35 U.S.C. § 102 should be withdrawn.

The Applicant respectfully points out that Kost fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant.

The Examiner also asserts:

"Kost discloses a communication system comprising a receiver for receiving analog signal; an analog to digital converter (46,50) for sampling the analog signal; and a DSP (54) adaptively determining a parallel-based compensation and a parallel-based operation to be performed to ensure a proper characteristic of the digital data (see fig.4 and 6). The parallel-based operation comprises adjusting an operation parameter of at least one A/D converter within the plurality of A/D converters. The parameter comprises at least one of gain, an offset and phase as claimed in claims 44, 46-51 (see col.1, lines 5-14 claims 1-22). The analog serial signal (45) is simultaneously fed to each A/D converters (46,50) as claimed in claim 52. The DSP provides control to each A/D converter as claimed in claims 53-54. The analog signal is partitioned into plurality of channel (45) before being fed to the plurality of A/D as claimed in claim 55. The receiver further comprises gain amplifiers (18) as claimed in claims 56-57. The analog to digital converter comprises a plurality of A/D (48,50) converters performing digital ampling of the incoming data signal as claimed in claim 119, 121. The analog data is partitioned into plurality of channels (45) each channel of the plurality of channels communicatively coupled to one A/D converter (48,50) and the analog signal is simultaneously fed to each A/D converter within the plurality of A/D converters as claimed in claims 123, 126-127." (office action, Part of Paper No./Mail Date 20070430, p. 5-6, emphasis added)

The Applicant respectfully points out that, within FIG. 1 of Kost, which depicts the "gain amplifiers (18)" is referred to as being a prior art embodiment with respect to Kost's disclosed novel subject matter. The Applicant respectfully points out that the "gain amplifiers (18)" of FIG. 1 of Kost (i.e., prior art with respect to Kost) do not appear in the novel embodiments which Kost refers to as his invention (e.g., within FIG. 2 and subsequent figures). Moreover, Kost goes on to teach and disclose that the elimination of the "operational amplifiers" (e.g., like the "operational amplifier 18" described within the prior art embodiment of FIG. 1 of Kost) within the novel embodiments which Kost refers to as his invention. In other words, the "operational amplifier 18" described within the prior art embodiment of FIG. 1 of Kost are wholly eliminated within FIG. 2 and

subsequent figures within Kost, as Kost explicitly teaches and discloses as also cited by the Applicant below.

Kost explicitly teaches and discloses:

"Accordingly, the present invention provides a new and improved method for the compensation of offset and gain errors in a wideband A/D interface which uses a plurality of converter components with interlaced outputs. It is an advantage of the present invention that it performs the necessary gain and offset adjustments after the signals have been converted to digital format, making it less expensive to produce since no analog gain and offset adjustment stage with attendant linear operational amplifiers and DACs are required. It is also an advantage of the present invention that elimination of the gain and offset adjustment stage used in prior art also eliminates the power consumption of that stage. It is a further advantage of the present invention that non linearities introduced by the prior art operational amplifiers are eliminated." (Kost, col. 4, lines 7-22, emphasis added)

Therefore, the Applicant respectfully believes that the "gain amplifiers (18)" of FIG. 1 of Kost to which the Examiner refers in rejecting certain of the Applicant's claimed subject matter is improper, as Kost does not teach and disclose that the "gain amplifiers (18)" are included within the same embodiment as FIG. 2 of Kost.

It is FIG. 2 of Kost that includes many other of the elements (e.g., "analog to digital converter (46,50)", the "DSP (54)" or the "digital signal conditioning stage (54)", the "analog serial signal (45)") to which the Examiner refers in rejecting certain of the Applicant's claimed subject matter.

In other words, the prior art embodiment of FIG. 1 of Kost (which includes the "gain amplifiers (18)" to which the Examiner refers) and the FIG. 2 of Kost (which includes many other of the elements, e.g., "analog to digital converter (46,50)", the "DSP (54)" or the "digital signal conditioning stage (54)", the "analog serial signal (45)") does not operate in accordance with one another. Therefore, the Applicant respectfully believes that it is improper to pick and choose elements from FIG. 1 and FIG. 2 of Kost (when the FIG. 1 and FIG. 2 do not operate with one another) in rejecting certain of the Applicant's claimed subject matter.

Moreover, it also appears that any correction/compensation performed in accordance with the tanning of Kost is performed wholly in the "digital signal conditioning stage (54)", and not within any other module that precedes or follows the "digital signal conditioning stage (54)".

In addition, in its corresponding ABSTRACT, Kost teaches and discloses:

"An apparatus for wide bandwidth analog to digital and digital to analog signal conversion is disclosed. An input/output stage (40) is coupled to an external analog system and includes reference voltages for calibration of the analog to digital (A/D) conversion process. A conversion stage (46), comprising a plurality of A/D converters (ADC) (48, 50) and a digital to analog converter (52), is coupled to the input/output stage and to a digital signal conditioning stage (54) which is coupled to an external digital system. Offset and gain errors in the outputs of each ADC are corrected by the application of appropriate correction parameters in the digital signal conditioning stage. The sampling intervals for each ADC are phased to allow the digital outputs of the ADCs to be interleaved and form a resulting digital data stream with a sampling rate a multiple of that of any one ADC." (Kost, ABSTRACT, emphasis added)

As can be seen, any correction/compensation performed in accordance with the tanning of Kost is performed "by the application of appropriate correction parameters in the digital signal conditioning stage". Clearly, Kost teaches and discloses that any detected "[o]ffset and gain errors in the outputs of each ADC are corrected by the application of appropriate correction parameters in the digital signal conditioning stage". The compensation is therefore not performed outside of the "digital signal conditioning stage", but rather within the "digital signal conditioning stage". The Applicant is unable to find any indication within Kost that any compensation is operable to be performed anywhere except within the "digital signal conditioning stage".

When characterizing Kost, the Examiner asserts that "[t]he DSP provides control to each A/D converter as claimed in claims 53-54" (see citation above from the office action).

The Applicant respectfully points out that, within FIG. 2 of Kost (which depicts the "analog to digital converter (46,50)", the "DSP (54)" or the "digital signal conditioning stage (54)", the "analog serial signal (45)"), there is no connectivity by

which the "DSP (54)" or the "digital signal conditioning stage (54)" is operable to provide any control to any of the "conversion stage 46" that includes the "analog to digital converter (46,50)".

The Applicant respectfully points out that there is only a one-way arrow connectivity between the "analog to digital converter (46,50)" and the "DSP (54)" or the "digital signal conditioning stage (54)" in FIG. 2 of Kost, and this is only from the "analog to digital converter (46,50)" to the "DSP (54)" or the "digital signal conditioning stage (54)". As such, the Applicant respectfully believes that this characterization of Kost by the Examiner is improper.

Again, the Applicant respectfully believes that it is in accordance with the teaching and disclosure of Kost that "[o]ffset and gain errors in the outputs of each ADC are corrected by the application of appropriate correction parameters in the digital signal conditioning stage", and Kost fails to teach and disclose any control provided from the "digital signal conditioning stage" to any "ADC" in Kost.

Moreover, Kost teaches and discloses:

"The digital signal conditioning stage 54 comprises a field programmable gate array (FPGA) device, a digital signal processor (DSP) and associated digital circuitry. Digital signal conditioning stage 54 performs the necessary activities of calibration, offset and gain adjustments, interleaving of the ADC outputs, and filtering of the resulting digital data stream. Although the preferred embodiment uses a FPGA device to accomplish the gain and offset correction, interlacing of ADC outputs, and filtering of the resulting digital data stream in the digital signal conditioning stage 54, the present invention is not limited in scope to the use of these devices. Those skilled in the art will recognize that any digital signal processing apparatus of equivalent capability may be used in place of the FPGA, with one example being a complex programmable logic device (CPLD)." (Kost, col. 5, lines 32-47, emphasis added)

Kost teaches and discloses that an "FPGA device to accomplish the gain and offset correction, interlacing of ADC outputs, and filtering of the resulting digital data stream in the digital signal conditioning stage 54" and also that "any digital signal processing apparatus of equivalent capability may be used in place of the FPGA", but

Kost does not appear to teach and disclose the use of any other module that is coupled to the "digital signal conditioning stage 54" to perform any compensation operation.

The Applicant is able only to find two feedback signals provided from the "DSP (54)" or the "digital signal conditioning stage (54)", and they are to the "digital to analog converter (52)" and to the "switching array 44" in FIG. 2 of Kost. These signals do not appear to be in accordance with performing any compensation operation, but rather to control "switches" (e.g., the operation of the "switching array 44") for use in "calibration".

Kost teaches and discloses:

"Reference voltages circuitry 60 in the references and switching array 44 of FIG. 3 produce four substantially constant value voltages, V.sub.2 through V.sub.5, used for calibrating the A/D conversion system." (Kost, col. 5, line 65 to col. 6, line 1, emphasis added)

Kost also teaches and discloses:

"The present invention possesses an analog output mode in which a digital data stream is supplied to the digital signal conditioning stage 54 by way of digital interface 57, and is further conveyed to the DAC 52 through data interface 51. The DAC 52 converts this digital data stream to a substantially equivalent analog signal 53 and supplies it to the switch array 62. When the appropriate command 55 is received by the switch control 64, switch S.sub.7 is closed and the switched analog signal 63 is supplied to the associated analog circuits." (Kost, col. 6, lines 31-40, emphasis added)

When considering the citation from Kost above as well as FIG. 2, FIG. 3, and FIG. 4 of Kost, the Applicant respectfully believes that the two feedback signals provided from the "DSP (54)" or the "digital signal conditioning stage (54)" (i.e., signal 51 provided to the "digital to analog converter (52)" and signal 55 provided to the "switching array 44") govern the operation of switches, and the Applicant respectfully believes that this does not appear to be not in accordance with performing any compensation parameter thereto as determined within the "DSP (54)" or the "digital signal conditioning stage (54)".

When considering the claims of Kost, it also appears to the Applicant that Kost clearly intends to perform any compensation within the "DSP (54)" or the "digital signal

conditioning stage (54)" disclosed therein, and not outside of the "DSP (54)" or the "digital signal conditioning stage (54)".

Kost teaches and discloses:

"1. An apparatus for use in wide bandwidth analog to digital conversion, comprising:

an input circuit for receiving an analog signal;

a plurality of analog to digital converters, each having an input coupled to an output of said input circuit, wherein said plurality of analog to digital converters convert analog signals appearing at outputs of said plurality of analog to digital signals to digital signals; and

a digital signal processor responsive to digital signals appearing at said outputs of said plurality of analog to digital converters, said digital signal processor including sum and multiplication means to apply offset and gain corrections to said digital signals and means for combining corrected digital signals at a single output." (Kost, claim 1, emphasis added)

Kost teaches and discloses:

"6. An apparatus for use in wide bandwidth analog to digital and digital to analog conversion, comprising:

an input/output circuit for receiving and sending analog signals;

a plurality of analog to digital converters, each having an input coupled to an output of said input/output circuit, wherein said plurality of analog to digital converters convert analog signals appearing at outputs of said plurality of analog to digital signals to digital signals;

a digital to analog converter having an input and an output, said output of said digital to analog converter being coupled to said input/output circuit; and

a digital signal processor having an interface for receiving and sending digital signals, said digital signal processor having an output coupled to said input of said digital to analog converter, said digital signal processor being responsive to said digital signals appearing at said outputs of said plurality of analog to digital converters, said digital signal processor including sum and multiplication means to apply offset and gain

corrections to said digital signals and means for combining corrected digital signals at a single digital output." (Kost, claim 6, emphasis added)

It appears to the Applicant that any compensation is performed exclusively within the "DSP (54)" or the "digital signal conditioning stage (54)" of Kost. The Applicant respectfully believes that Kost teaches and discloses that any compensation operation is performed exclusively within the "DSP (54)" or the "digital signal conditioning stage (54)".

As such, the Applicant respectfully believes that Kost fails to teach and disclose any performing of any compensation operation outside of the "DSP (54)" or the "digital signal conditioning stage (54)". The Applicant also respectfully believes that Kost fails to teach and disclose any performing of any compensation operation outside of the "DSP (54)" or the "digital signal conditioning stage (54)" as well.

As such, the Applicant respectfully believes that Kost fails to teach and disclose any selectivity of performing any compensation operation by the digital signal processor or by at least one additional module that is coupled to the digital signal processor.

Therefore, in light of at least these comments made above, the Applicant respectfully believes that Kost fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant in each of independent claims indicated above that the Examiner rejects as being anticipated by Kost.

The Applicant also respectfully believes that the dependent claims indicated above that the Examiner rejects as being anticipated by Kost, being further limitations of the subject matter as claimed in allowable independent claims are also allowable.

As such, in light of at least these comments made above, the Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-8, 12-27, 34, 37-41, 113, 116-117, 119, 121, 123, 126-127, 134-141, 145-146-160, 163, 167, 170-175, 178, 183, 184 under 35 U.S.C. § 102(b) as being anticipated by Kost.

5. In the office action, the Examiner states:

"Claims 42-57, 62-69, 76-79, 113-128, 176, 177, 179-182 are rejected under 35 U.S.C. 102(b) as being anticipated by Kost et al. (6,081,215)." (hereinafter referred to as "Kost") (office action, Part of Paper No./Mail Date 20070430, p. 5).

The Applicant respectfully traverses.

The Applicant has amended certain of the claims.

The Applicant respectfully points out that, in order to support a proper rejection under 35 U.S.C. §102, a singular reference must teach and disclose each and every limitation of the subject matter as claimed by the Applicant. If the singular reference fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant, the rejections under 35 U.S.C. § 102 should be withdrawn.

The Applicant respectfully points out that Kost fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant.

The comments made above with respect to Kost are also applicable here.

It appears to the Applicant that any compensation is performed exclusively within the "DSP (54)" or the "digital signal conditioning stage (54)" of Kost. The Applicant respectfully believes that Kost teaches and discloses that any compensation operation is performed exclusively within the "DSP (54)" or the "digital signal conditioning stage (54)".

As such, the Applicant respectfully believes that Kost fails to teach and disclose any performing of any compensation operation outside of the "DSP (54)" or the "digital signal conditioning stage (54)". The Applicant also respectfully believes that Kost fails to teach and disclose any performing of any compensation operation outside of the "DSP (54)" or the "digital signal conditioning stage (54)" as well.

As such, the Applicant respectfully believes that Kost fails to teach and disclose any selectivity of performing any compensation operation by the digital signal processor or by at least one additional module that is coupled to the digital signal processor.

Therefore, in light of at least these comments made above, the Applicant respectfully believes that Kost fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant in each of independent claims indicated above that the Examiner rejects as being anticipated by Kost.

The Applicant also respectfully believes that the dependent claims indicated above that the Examiner rejects as being anticipated by Kost, being further limitations of the subject matter as claimed in allowable independent claims are also allowable.

As such, in light of at least these comments made above, the Applicant respectfully requests that the Examiner withdraw the rejection of claims 42-57, 62-69, 76-79, 113-128, 176, 177, 179-182 under 35 U.S.C. § 102(b) as being anticipated by Kost.

Claim Rejections - 35 U.S.C. § 103

7. In the office action, the Examiner states:

"Claims 9-11, 28-33, 59-61, 72-75, 142-144, 161-162, 164-166 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kost in view of Stewart (5,671,253)." (hereinafter referred to as "Kost" and "Stewart", respectively) (office action, Part of Paper No./Mail Date 20070430, p. 6).

The Applicant respectfully traverses.

The Applicant has amended certain of the claims.

The comments made above with respect to Kost are also applicable here.

Dependent claims 9-11, 28-33 depend (directly or indirectly) from independent claim 1.

Dependent claims 59-61, 72-75 depend (directly or indirectly) from independent claim 42.

Dependent claims 142-144, 164-166 depend (directly or indirectly) from independent claim 134.

The Applicant respectfully believes that independent claims 1, 42, and 134 are allowable over Kost.

The Applicant respectfully believes that the inclusion of Stewart with Kost does not overcome the deficiencies of Kost with respect to at least the comments provided above.

Therefore, the Applicant respectfully believes that independent claims 1, 42, and 134 are allowable over Kost in view of Stewart.

The Applicant also respectfully believes that the dependent claims indicated above that the Examiner rejects as being unpatentable over Kost in view of Stewart, being further limitations of the subject matter as claimed in allowable independent claims are also allowable.

As such, in light of at least these comments made above, the Applicant respectfully requests that the Examiner withdraw the rejection of claims 9-11, 28-33, 59-61, 72-75, 142-144, 161-162, 164-166 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kost in view of Stewart.

Allowable Subject Matter

97. In the office action, the Examiner states:

"Claims 80-112 and 129-133 are allowed." (office action, Part of Paper No./Mail Date 20070430, p. 7).

The Applicant respectfully agrees with the Examiner that claims 80-112 and 129-133 are allowable.

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The Applicant respectfully believes that claims 1-184 are in condition for allowance and respectfully requests that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present U.S. utility patent application.

RESPECTFULLY SUBMITTED.

By: /SXShort/ Reg. No. 45,105

Shayne X. Short, Ph.D., Reg. No. 45,105
Direct Phone: (512) 825-1145
Direct Fax No. (512) 394-9006

GARLICK HARRISON & MARKISON
ATTORNEYS AT LAW
P.O. BOX 160727
AUSTIN, TEXAS 78716-0727
TELEPHONE (512) 825-1145 / FACSIMILE (512) 394-9006 OR (512) 301-3707